IN THE SPECIFICATION

Please amend the paragraph starting on page 1, line 32 of the specification as follows:

A second known architecture, called an "Anti-Jitter Circuit" uses a first fixed-width pulse generator controlled by the signal from the phase accumulator, a charge pump that charges and discharges a capacitor, a comparator, and a second pulse generator controlled on the falling edges of the comparator. Since the duration of the pulse set by the signal from the phase accumulator is fixed, the instants of occurrence of the output pulse are equidistant, even if the edges at its input are not. The period thus obtained corresponds to the average period of the signal from the phase accumulator.

A third known architecture consists in using a clock generator with N phases, where N is a whole number, at the average frequency Fout of the phase accumulator overflow bit. At each overflow of the phase accumulator, that one of the N phases is chosen that enables the average period 1/Fout of the accumulator overflow bit to be matched as closely as possible. An example of such an architecture is given in the article "A Virtual Clock Enhancement Method for DDS Using an Analog Delay Line", R. Richter, H.J. Jentschel, IEEE Journal of Solid State Circuits, Vol. 36, No 7, July 2001. The generator includes a loop of delay elements called a Delay-Locked Loop or DLL. Each delay element consists of an inverter.